Amendments to the Specification:

Please replace the paragraph beginning at page 9, line 8 with the following amended paragraph:

--Fig. 2 is a truth table showing operation examples of a shift circuits A to E ~~and sort circuits A to D of the embodiment~~;--

Please replace the paragraph beginning at page 9, line 10 with the following amended paragraph:

--Fig. 3 is a truth table showing operation examples of sort circuits A to C ~~shift circuits B to D of the embodiment~~;--

Please replace the paragraph beginning at page 9, line 12 with the following amended paragraph:

--Fig. 4 is a truth table showing operation examples in an enable state of sort circuits D to F ~~one-bit shift circuits A to C of the embodiment~~;--

Please replace the paragraph beginning at page 13, line 24 with the following amended paragraph:

-- In signals inputted to the second sort part 7, the signals sampled every m bits as BIT 0, BIT m, BIT 2m, $\cdots$, BIT (n-1) $\cdot$ m are inputted to the delay circuit 10. Also, signals in which the signals inputted to the delay circuit 10 are shifted by one bit as BIT 1, BIT (m+1), BIT (2m+1), $\cdots$, BIT ((N-1) $\cdot$ m+1) are inputted to the next sort circuit 11a. Similarly, ~~signals in which the~~ signals inputted to the sort circuit 11a are shifted by one bit ~~are~~ and inputted to the sort circuit 11b, and ~~signals in which the~~ signals inputted to the sort circuit 11b are further shifted by one bit ~~are~~ and inputted to the sort circuit 11c.--

Amendments to the Claims: